MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2017/2018

EEN1036 –DIGITAL LOGIC DESIGN

(TE/RE)

17 MARCH 2018
2.30 p.m. – 4.30 p.m.
(2 Hours)

INSTRUCTION TO STUDENTS

1. This question paper consists of 6 pages (including cover page) with 4 Questions only.

2. Attempt **ALL FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please write all your answers in the Answer Booklet provided.

Question 1

(a) Convert the following numbers from the given base to the other three bases listed in the table

Decimal	Binary	Octal	Hexadecimal
			FF1
		771	
120.5			

[9 marks]

(b) Complete the following table for unsigned binary numbers, and perform each subtraction in the 2's complement form

A_2	A_{10}	B_2	B_{10}	$(A+B)_2$	$(A-B)_2$	$(A \times B)_2$
1011		1011				
00110		0111				

[11 marks]

(c) Convert the following binary numbers to hexadecimal numbers and perform the addition in hexadecimal form.
X = 100010101011; Y = 101101111000

[5 marks]

Continued...

Question 2

(a) Prove the following expressions:

(i) $Q = A.B.\overline{C} + A.\overline{C} + \overline{A}.\overline{C}.D + \overline{A}.\overline{C}.\overline{D} = \overline{C}$

[6 marks]

(ii) $Q = A.B.(\overline{B} + C) + B.C + B = B$

[6 marks]

(b) Use Karnaugh map techniques to simplify

$$Y = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}.B.\overline{C}.\overline{D} + \overline{A}.B.\overline{C}.D$$ [3 marks]

(c) Draw the logic circuit diagram for the following Boolean expression, and construct the truth table of Z. Then simplify Z

$Z = A.B\left(B.\overline{C} + \overline{B}.C + \overline{A}.B\right)$

[10 marks]

Continued...

Question 3

(a) A sequential circuit with the state table as shown in Table Q3A is given, where X, Y and Z are the states with I as state input and O as state output.

Table Q3A

Present State	Next State		Output, O	
	$I=0$	$I=1$	$I=0$	$I=1$
X	X	Z	1	1
Y	X	Z	0	1
Z	Z	Y	0	0

i) Draw the state diagram based on the state table as shown in Table Q3A

[7 marks]

ii) Given the input sequence of I = 110100, determine the output sequence of O together with the states if initial state is X.

[6 marks]

(b) Figure Q3B shows the 8-bits shift register counter. Complete the following table based on the configuration as shown in the shift registers. Each row in the table indicates one clock cycle of the shift pulse.

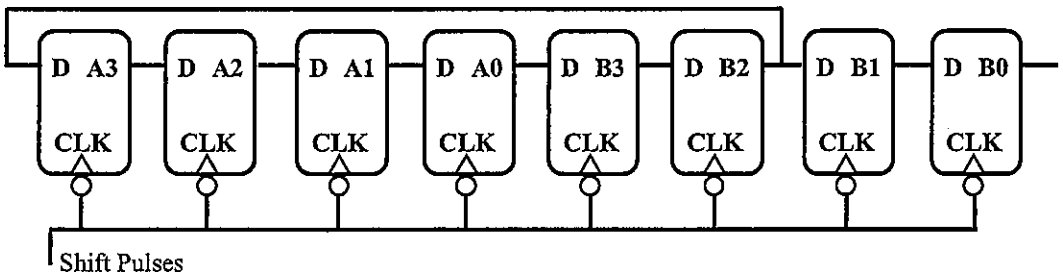

Figure Q3B

A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0
1	1	1	0	0	0	0	0
0	1	1	1	0	0	0	0

[6 marks]

Continued...

(c) A 555 timer module with the circuit configuration as astable multivibrator is given in Figure Q3C. Calculate the duty cycle (in %) and the frequency (in kHz) of the oscillator.

[6 marks]

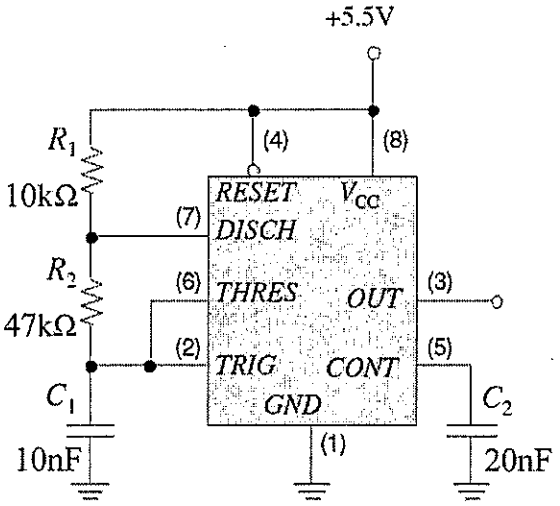

Figure Q3C

Continued...

Question 4

(a) Realize the following pair of expressions by using the mentioned logic gates with active high output 3-to-8 line decoder.

$$g_1(y_2, y_1, y_0) = \sum m(0,1,7) \text{ by using OR gate}$$
$$g_2(y_2, y_1, y_0) = \sum m(1,3,5,7) \text{ by using NOR gate}$$

[5 marks]

(b) Given two signed numbers, $+93_{10}$ and $+87_{10}$. Perform binary addition operation on both numbers by using 8-bits register. Justify is there any arithmetic overflow occur in the operation. Elaborate your answer.

[4 marks]

(c) Implement the expression $f_1(X, Y, Z) = \sum m(0,1,3,6)$ by using 4-to-1 multiplexer. Pick only Z as the data input.

[6 marks]

(d) Find the minimal SOP expression for a comparator that compares two binary numbers $X=X_1X_0$ and $Y=Y_1Y_0$. The output signal Z is set to 1 if X is greater than Y, otherwise Z is cleared to 0.

[10 marks]

End of Page